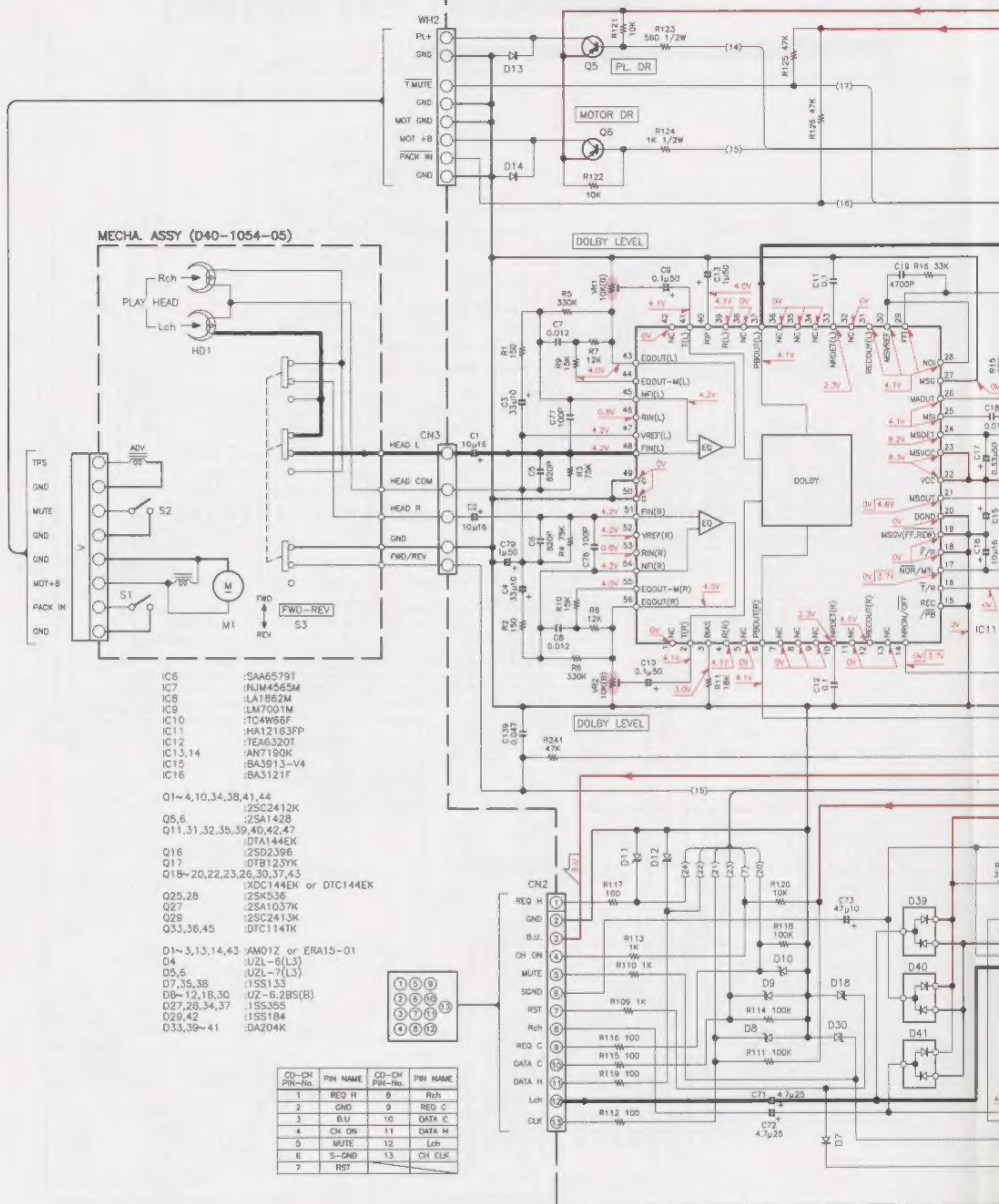


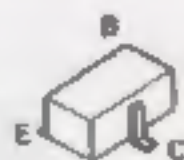
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2SD2396



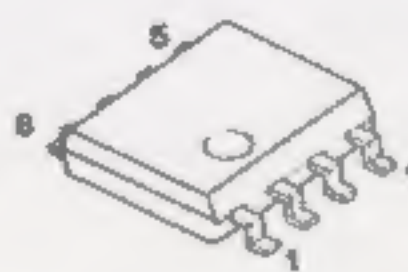
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DTA144EK	2SA1036K
DTB123YK	2SA1037K
DTC114TK	2SC2412K
DTC144EK	2SC2413K
XDA124EK	



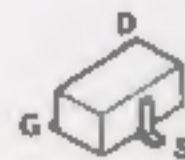
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2SB1326

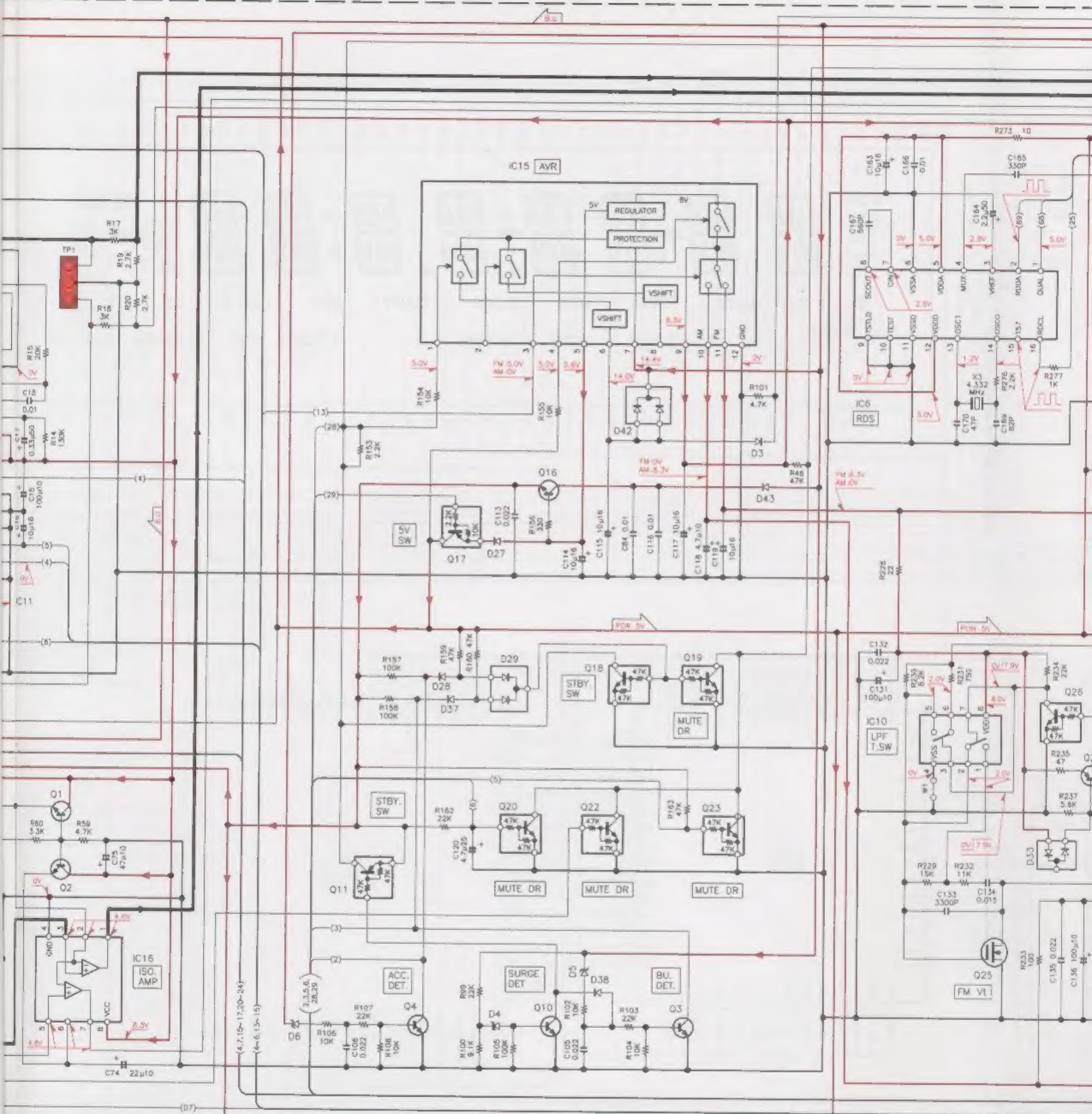


NJM4565M



2SK536





LC3564QM-10

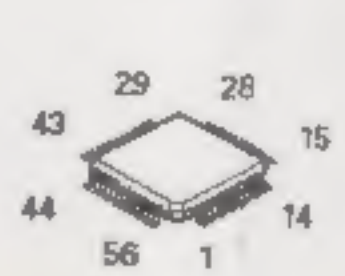
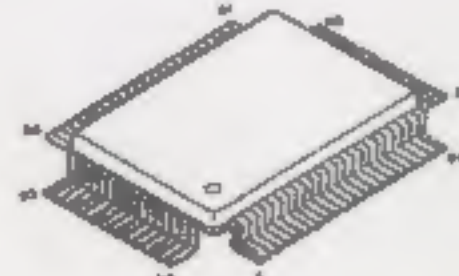
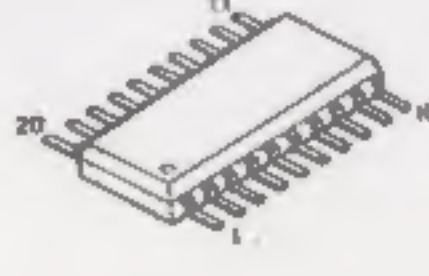
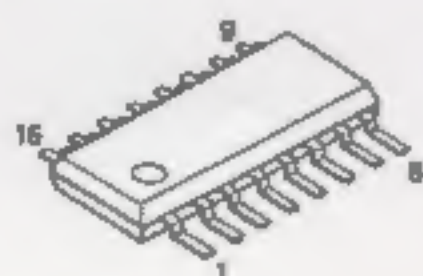
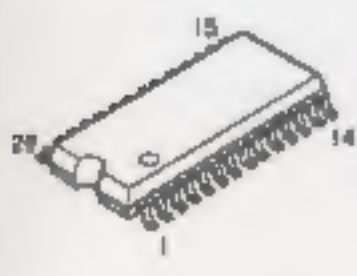
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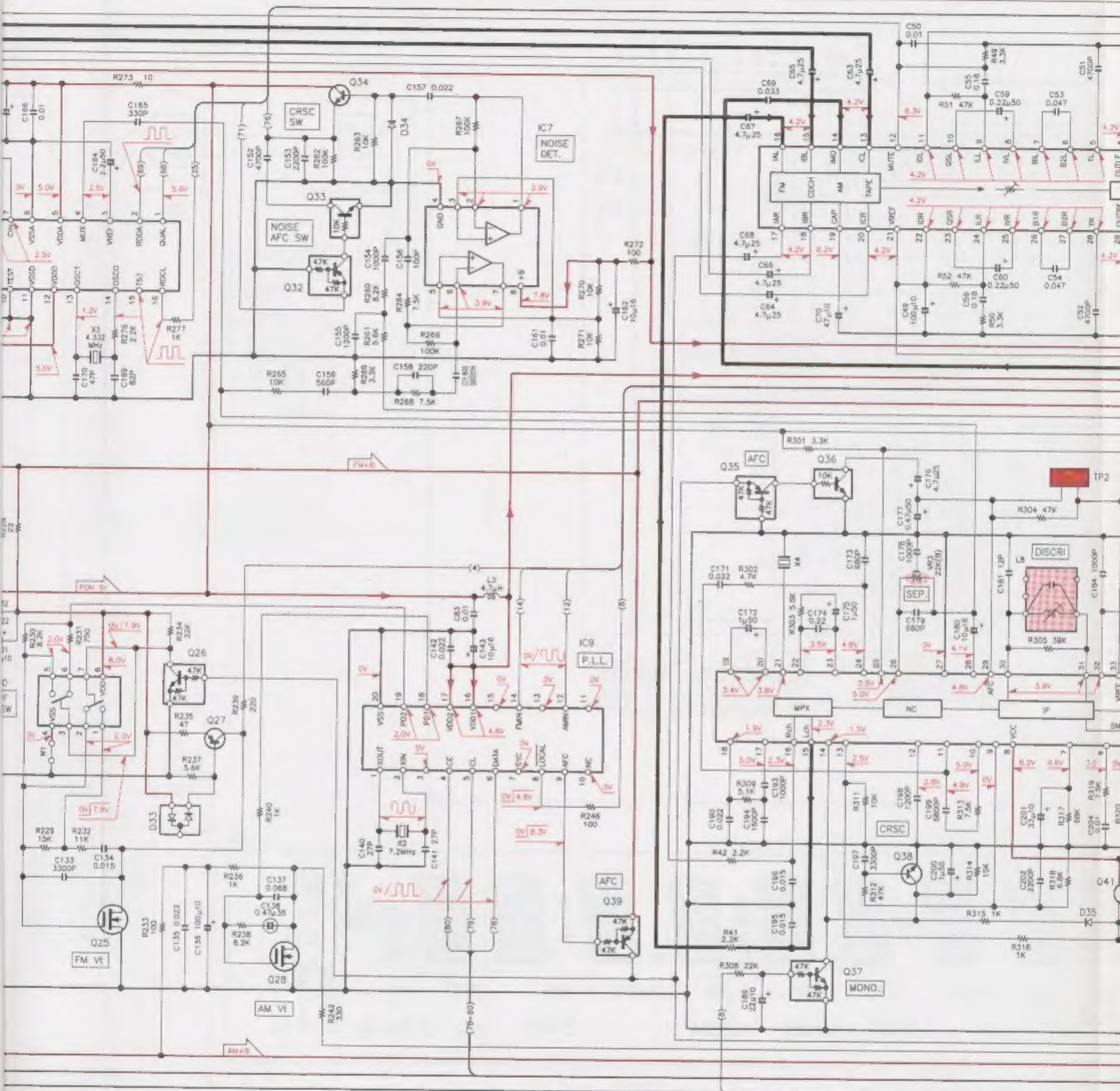
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LM7001M

M38067M8D123FP

HA12163FP





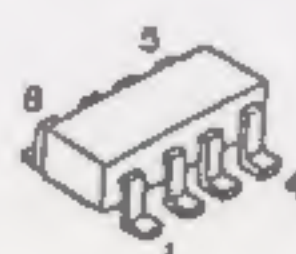
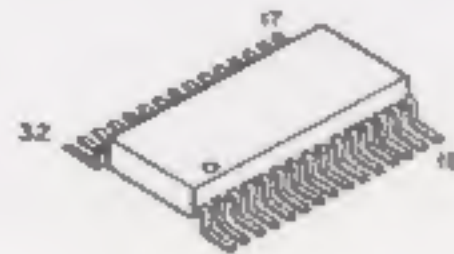
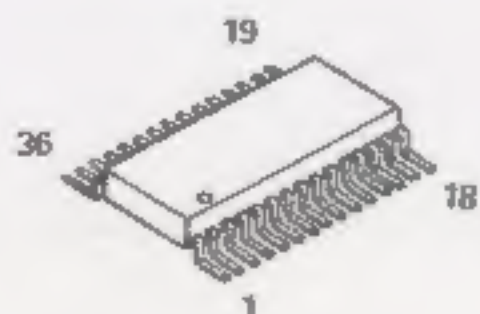
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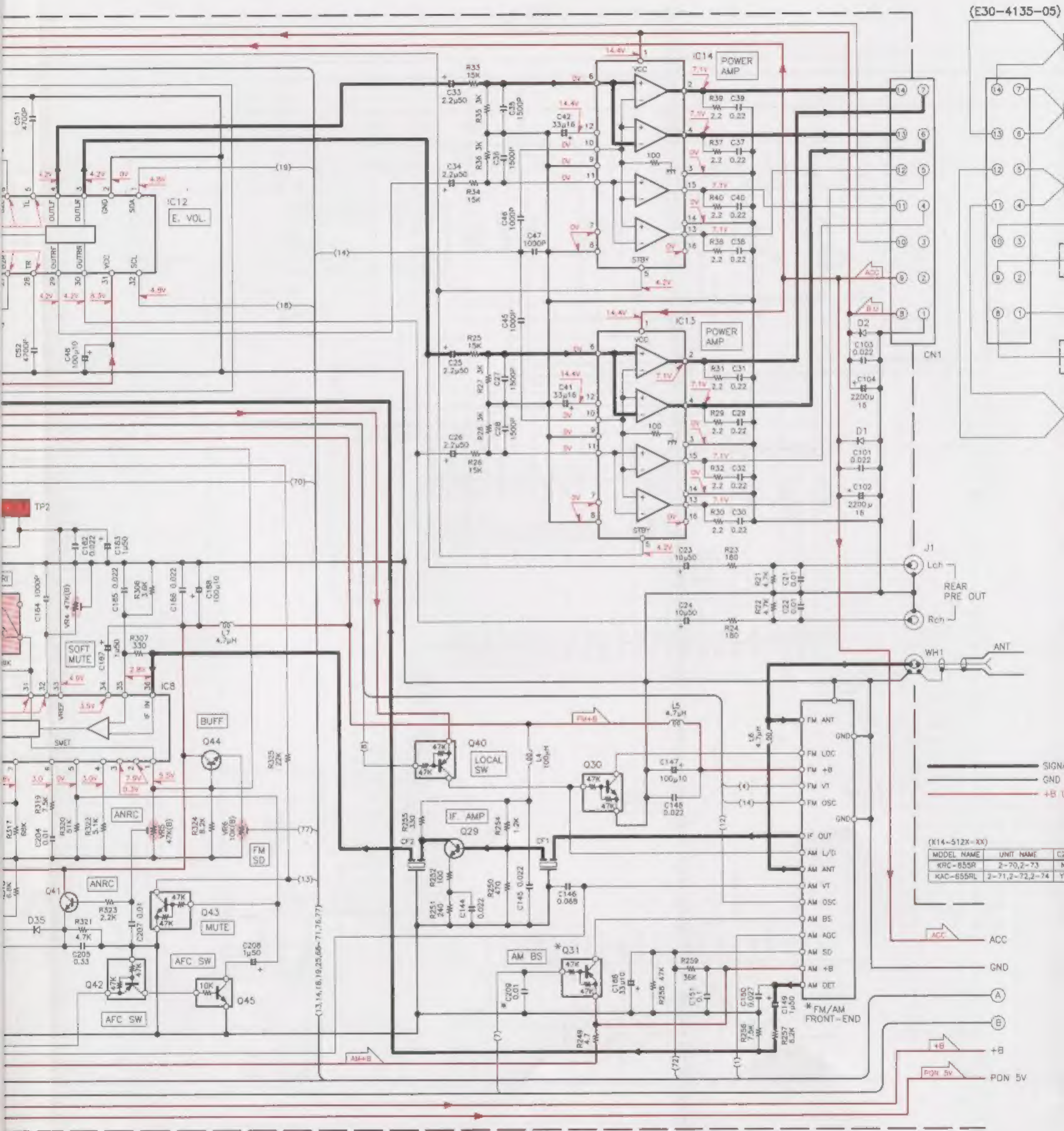
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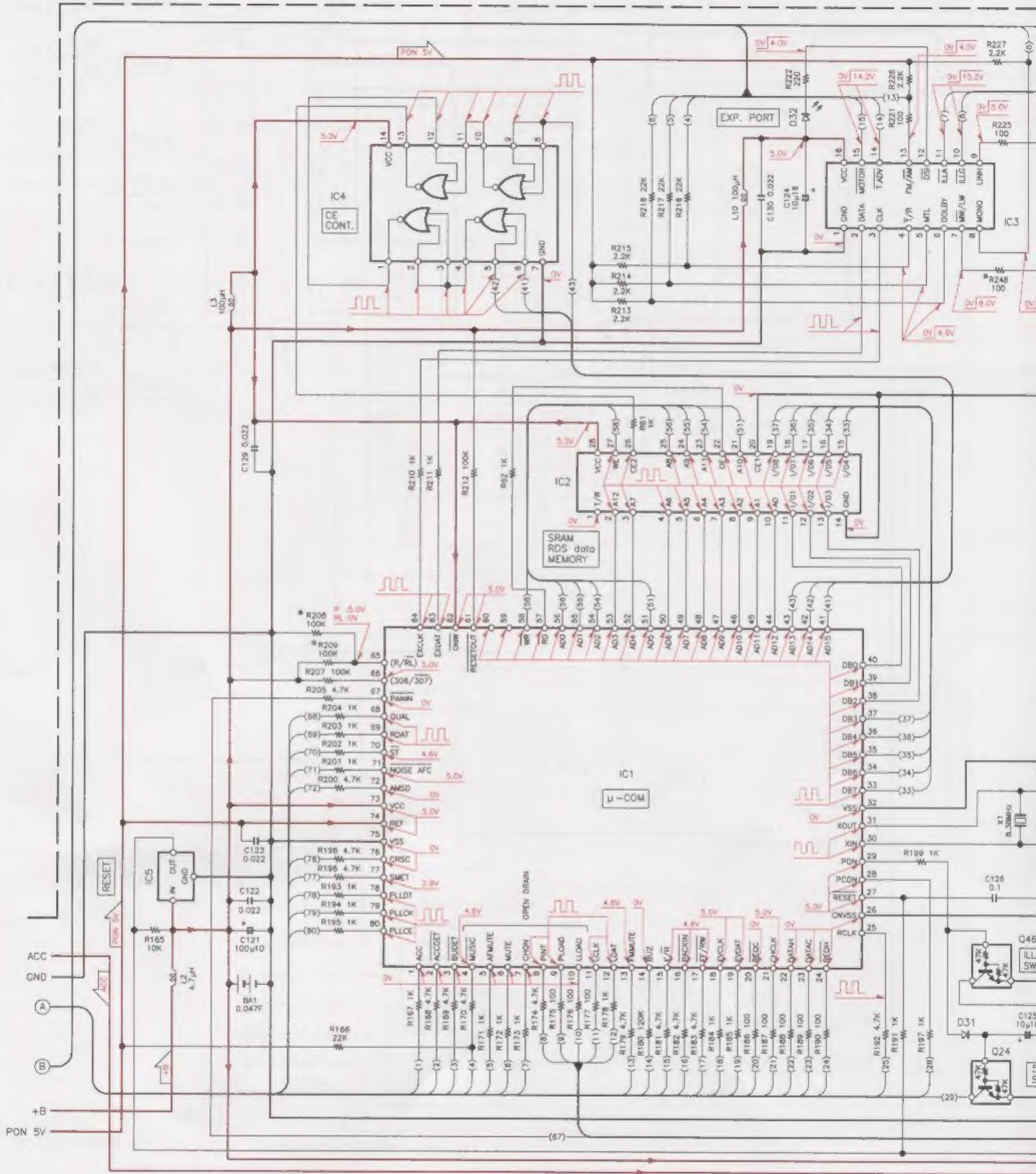
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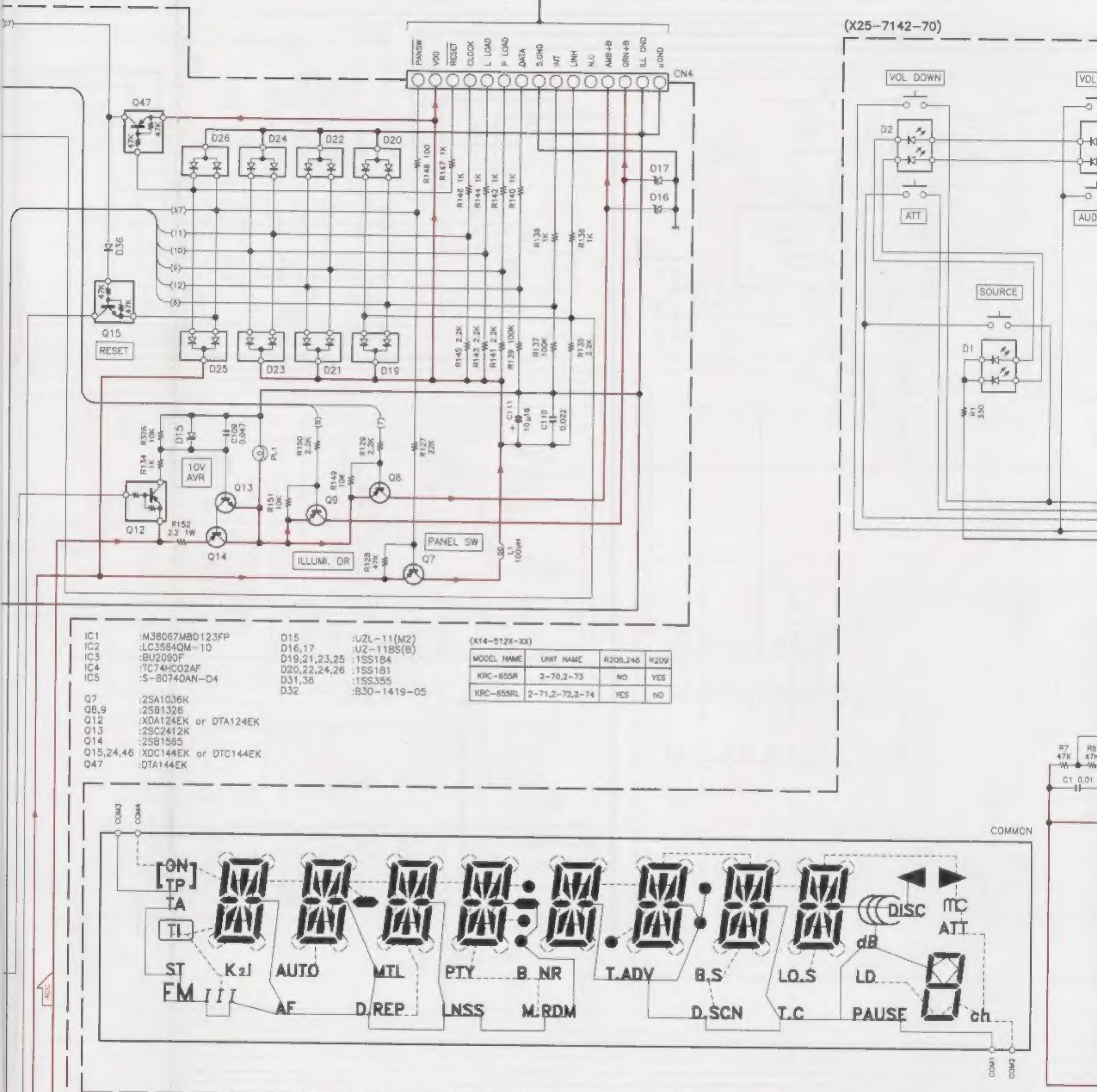
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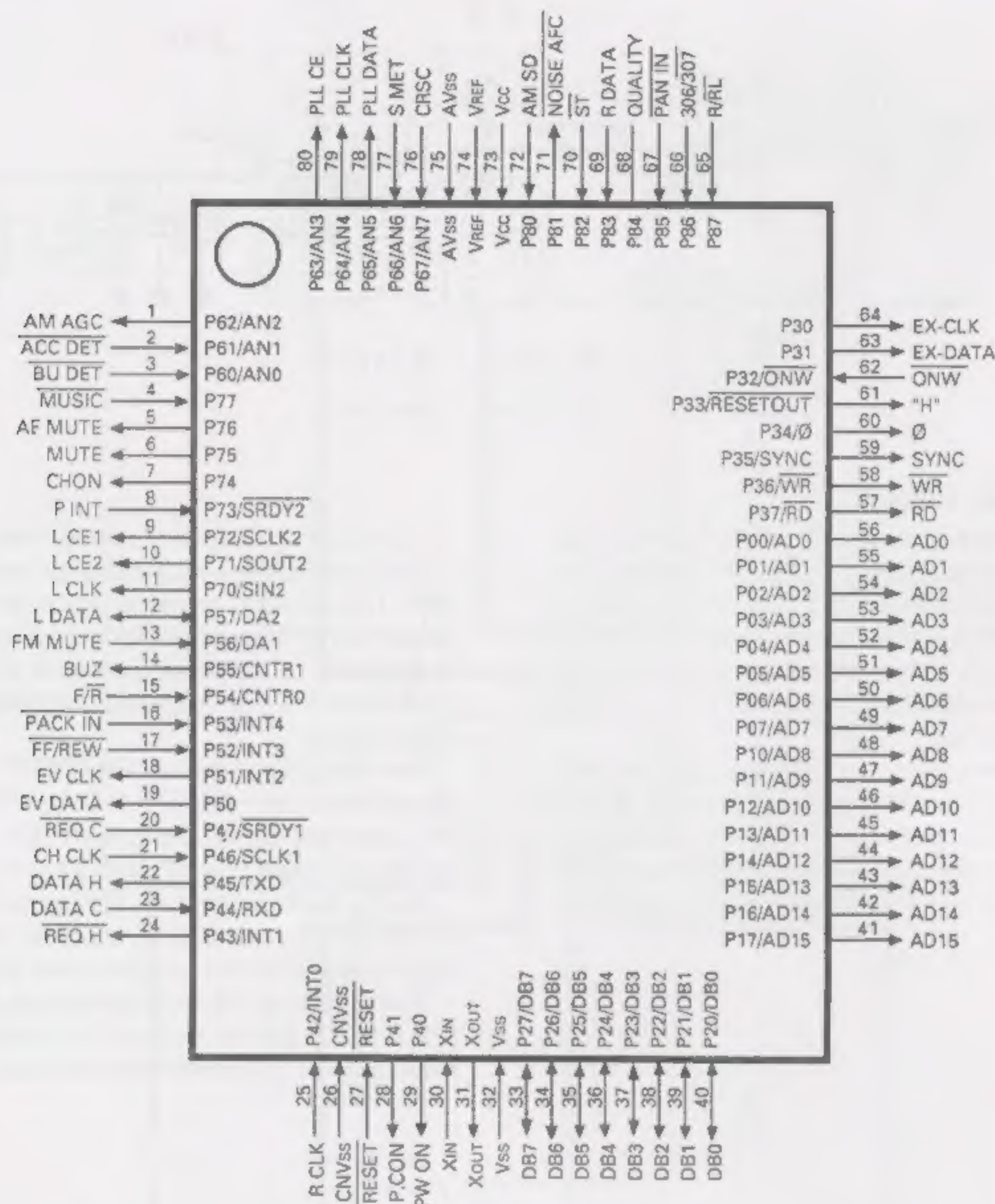


KRC-655R/RL

CIRCUIT DESCRIPTION

IC1 : M38067M8D123FP (X14-)

• Pin connection



• Pin function

No.	Port name	I/O	Signal name	Function	Active status
1	P62/AN2	O	AM AGC	AM AGC	AM SEEK
2	P61/AN1	I	ACC DET	ACC power supply	ACC OFF
3	P60/AN0	I	BU DET	Back-up power supply	Back-up OFF
4	P77	I	MUSIC	Music signal (Used for detection of blank between tunes)	Music detected
5	P76	O	AF MUTE	Muting (Used in AF search)	
6	P75	O	MUTE	Muting	
7	P74	O	CHON	CD-CH ON	
8	P73/SRDY2	I	P INT	LCD driver MSM6606 end of A key scan cycle	
9	P72/SCLK2	O	L CE1	LCD driver MSM6606 Latch	
10	P71/SOUT2	O	L CE2	LCD driver MSM6544 Latch	

CIRCUIT DESCRIPTION

No.	Port name	I/O	Signal name	Function	Active status
11	P70/SIN2	O	L CLK	LCD driver Clock	
12	P57/DA2	I/O	L DATA	LCD driver Data	
13	P56/DA1	I	FM MUTE	FM band muting	FM station detected
14	P55/CNTR1	O	BUZ	Buzzer	
15	P54/CNTR0	I	F/R	Tape direction Forward/Reverse	H=Forward
16	P53/INT4	I	PACK IN	Tape pack in	Pack in
17	P52/INT3	I	FF/REW	Tape fast winding (FF/REW)	FF/REW
18	P51/INT2	O	EV CLK	Electronic Volume TEA6320 Clock	
19	P50	O	EV DATA	Electronic Volume TEA6320 Data	
20	P47/SRDY1	I	REQ C	CD-CH Request CD-CH	
21	P46/SCLK1	I	CH CLK	CD-CH CLOCK	
22	P45/TXD	O	DATA H	CD-CH Data Head unit	
23	P44/RXD	I	DATA C	CD-CH Data CD-CH	
24	P43/INT1	O	REQ H	CD-CH Request Head unit	
25	P42/INT0	I	R CLK	RDS Clock	
26	CNVss	I	CNVss	μ-com chip operation control mode switching	CNVss=GND
27	RESET	I	RESET	Hardware Reset	Active "L"
28	P41	O	P.CON	Power control	
29	P40	O	PW ON	Power ON +5V	
30	XIN	I	XIN	Clock input	
31	XOUT	O	XOUT	Clock output	
32	Vss	I	Vss	Power supply input	Vss=GND
33~40	P27/DB7~P20/DB0	I/O	DB7~DB0	S-RAM Data Bus 7~0	
41~48	P17/AD15~P10/AD8	O	AD15~AD8	S-RAM Address 15~8	
49~56	P07/AD7~P00/AD0	O	AD7~AD0	S-RAM Address 7~0	
57	P37/RD	O	RD	S-RAM Read control	
58	P36/WR	O	WR	S-RAM Write control	
59	P35/SYNC	O	SYNC	Outputs 'H' for 1 period of ■ during op-code fetching. (Not used)	
60	P34/φ	O	φ	Internal system clock φ output. (Not used)	
61	P33/RESETOUT	O	'H'	Permanently outputs "H". (Not used)	
62	P32/ONW	I	ONW	Delays internal system clock φ by half. (Not used)	
63	P31	O	EX DATA	Serial parallel Extension port IC Data	
64	P30	O	EX CLK	Serial parallel Extension port IC Clock	
65, 66	P87, P86	I	R/RL, 306/307	Destination setting (Read only during reset-start).	L=RL, L=307
67	P85	I	PAN IN	Panel Attached/Detached	Panel attached
68	P84	I	QUALITY	RDS Quality	
69	P83	I	R DATA	RDS Data	
70	P82	I	ST	FM Stereo/Mono	Stereo
71	P81	O	NOISE AFC	RDS Noise AFC	
72	P80	I	AM SD	AM SD	AM station detected
73	Vcc	I	Vcc	Power supply input	Vcc=+5V
74	VREF	I	VREF	Reference power for A/D converter. Analog Max. voltage.	VREF=+5V
75	AVss	I	AVss	Analog power input for A/D converter. Analog Min. voltage.	AVss=GND
76	P67/AN7	I	CRSC	FM noise (Used by A/D)	
77	P66/AN6	I	S MET	FM S-meter (Used by A/D)	
78	P65/AN5	O	PLL DATA	PLL LM7001M Data	
79	P64/AN4	O	PLL CLK	PLL LM7001M Clock	
80	P63/AN3	O	PLL CE	PLL LM7001M Chip Enable	